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Microstructure and electrical properties of ferroelectric $Pb(Zr_{0.53}Ti_{0.47})O_3$ films on Si with TiO_2 buffer layers

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Abstract. $Pb(Zr_{0.53}Ti_{0.47})O_3$ (PZT) thin films were prepared on p-type Si(100) substrates with TiO_2 buffer layers. Both the PZT films and TiO_2 buffer layers were deposited by the pulsed laser deposition technique using a KrF excimer laser. The depth profile of the constituent elements observed by Auger electron spectrometry (AES) showed that TiO_2 buffer layers effectively prevented interdiffusion between PZT and Si substrates. The capacitance–voltage (C–V) characteristics of the Pt/PZT/TiO_2/Si structures exhibited ferroelectric switching properties and a memory window of about 2.0 V at an applied voltage of 6.0 V.

1. Introduction

Recently, ferroelectric materials such as $Pb(Zr_{0.53}Ti_{0.47})O_3$ (PZT) have been extensively studied for dynamic random access memory (DRAM) and nonvolatile memory applications [1, 2]. In particular, the ferroelectric field-effect transistors (ferroelectric FETs), in which the gate with metal/ferroelectric/semiconductor (MFS) structure is controlled by the spontaneous polarization of ferroelectric materials are expected to be one of the leading candidates for future nonvolatile memory devices [3], because of their fast switching speed, nonvolatility, tolerance against radiation and high integrated density. In order to realize ferroelectric FETs, preparation of ferroelectric/Si structures with a sharp interface is essential. However, it is very difficult to deposit the ferroelectric PZT films directly on silicon substrates without interfacial reaction, because Pb is highly reactive with Si and easily diffuses into the Si substrates. Therefore, an insulating buffer layer preventing interdiffusion of Si and Pb is necessary for PZT film deposition on Si substrates. Thus many kinds of buffer layer such as yttrium stabilized zirconia (YSZ) [4], CeO_2 [5], MgO [6] and $SrTiO_3$ [7] films have been proposed for the suppression of the diffusion at the interface between ferrroelectric materials and Si substrates. But it was found that devices with these buffer layers have large absorption currents due to the high density of crystalline defects or carrier traps existing in the interface of Si and buffer [8]. So selecting a suitable buffer layer and corresponding processing conditions is still essential to improve the performance of ferroelectric FETs.

In this study, a buffer layer of TiO_2 was used for $Pb(Zr_{0.53}Ti_{0.47})O_3$ (PZT) growth on Si substrates by pulsed laser deposition (PLD). We expected that the thin TiO_2 films formed by PLD would serve as a diffusion barrier and result in a high quality TiO_2/Si interface with low interface trap density. The crystalline properties for the PZT/TiO_2/Si structure and its electrical properties will also be presented.

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2. Experiment

The substrates with a dimension of 1 cm × 1 cm were cut from the (100) oriented n-type silicon wafers with 4–5 Ω cm resistivity and 500 μm thickness. They were degreased and sequentially boiled in $NH_4OH/H_2O_2/H_2O$ (1:1:5) solution followed by dipping in diluted HF and rinsing with deionized water. Then, the substrates were soaked in a hot solution of $HCl/H_2O_2/H_2O$ (3:1:1) followed by dipping in a diluted HF solution to remove the surface oxide layer.

Both TiO_2 buffer layers and PZT thin films were deposited by PLD. A KrF excimer laser, operating at a wavelength of 248 nm and at pulse duration of 30 ns, was used. Targets used for deposition of TiO_2 layers were 1.5 centimetre diameter polycrystalline TiO_2 targets fabricated by sintering cold pressed TiO_2 powder pellets at 1400 °C for 10 h in air. Those for PZT films were made by conventional solid state reaction. The starting materials including ZrO_2, TiO_2 and excess PbO were ball milled for 24 hours, and preheated at 800 °C for 5 hours in air. The pellets pressed under 18 MPa pressure were sintered at 1100 °C for 2 hours.

The laser beam of 200 mJ average pulse energy was focused at a 45° angle onto the target by an ultraviolet grade plano-convex lens. The repetition rate was fixed at 5 Hz for both TiO_2 layers and PZT films. The laser fluence was maintained at 2.0–2.5 J cm^{-2} by adjusting the lens-to-target distance. The TiO_2 and PZT targets were mounted on the same target holder at the same time for the *in situ* multilayer deposition by PLD. The Si substrate was placed on a metal substrate stage parallel to the target at a distance of 40 mm. Before deposition, the growth chamber was first evacuated to a base pressure of about 5×10^{-4} Pa using a turbomolecular pump. At the base pressure the TiO_2 films were deposited at room temperature for 30 s, followed by a deposition at 700 °C and 15 Pa O_2 pressure for 90 s. The total thickness of the TiO_2 layer obtained this way was around 50 to 60 nm. In order to improve the electrical properties of TiO_2/Si structures, as-grown TiO_2 thin films on Si substrates were annealed *in situ* at 750 °C in an oxygen atmosphere for 30 min. After the annealing, PZT films 300 nm thick were deposited at a deposition rate of about 20 nm min^{-1} at 30 Pa O_2 pressure and substrate temperature 650 °C followed by annealing at the same temperature and 0.6 atm O_2 pressure for 10 minutes in the same chamber. During deposition, the substrates and target rotated at a speed of 8 and 15 rpm, respectively, to achieve a uniform temperature distribution on the substrate, and a uniform ablation rate on the target and eventually uniform film growth on the substrates. For electrical measurements, the top platinum electrodes having a diameter of 200 μm were deposited on PZT film using a shadow mask at room temperature by PLD. Platinum films were also deposited on the back surface of Si as the back electrode. Prior to Pt deposition, the native Si oxide was removed by a standard HF etching. After the electrode formation, annealing at 400 °C in an oxygen atmosphere was carried out for 30 min in order to obtain the ohmic contact.

X-ray diffraction (XRD) with Cu Kα measurement was performed to investigate the crystallographic structure of the PZT/TiO_2/Si structure. Auger electron spectrometry (AES) was applied to study interdiffusion of constituent elements. Polarization–electric field (P–E) and capacitance–voltage (C–V) measurements were employed to study its electrical properties.

3. Results and discussion

PZT films generally have two types of structure, i.e. the perovskite phase showing ferroelectricity and the pyrochlore phase showing no ferroelectricity. The former is commonly crystallized at higher temperatures than the latter. Figure 1 shows the x-ray diffraction patterns using Cu Kα radiation for our PZT films formed on the above-mentioned TiO_2 buffer layers. Diffraction peaks originating prominently from the (101), (111) and (211) perovskite PZT

planes are observed at 2θ of 31.0, 38.2 and 55.0° respectively, in addition to those due to substrates and platinum electrodes, and no pyrochlore phase could be observed. The appearance of weak peaks around 29 and 34° could be due to a small amount of the excess PbO_2.

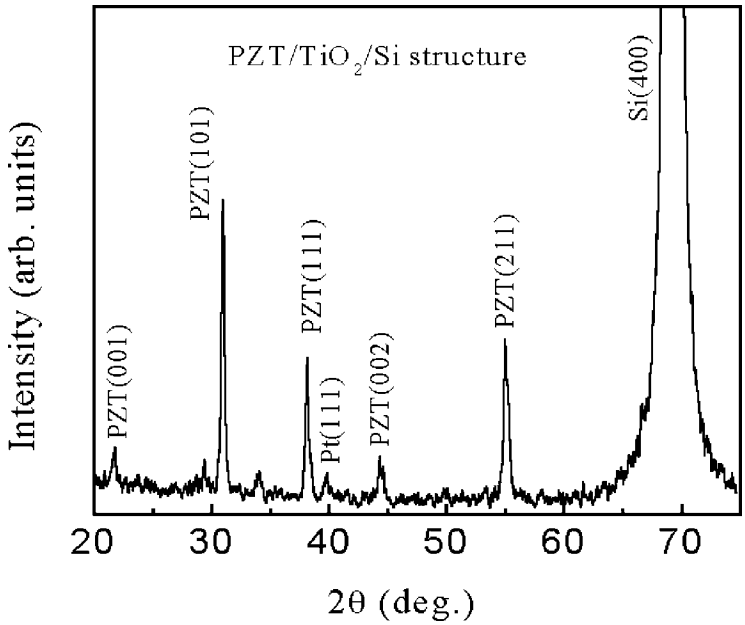

Figure 1. X-ray diffraction patterns (Cu Kα) of PZT/TiO_2 structures deposited on p-Si(100) substrates by PLD.

To investigate the effect of deposition temperature for PZT, we have tried different deposition temperatures from 400 to 800 °C. The XRD patterns (not shown here) indicate that at temperatures lower than 500 °C, the films are amorphous. When the temperature is between 500 and 750 °C, other phases such as the pyrochlore phase PZT, ZrO_2 and Ti_3O_5 appear. However, when the temperature is higher than 750 °C, the serious volatility of Pb results in weakness of the XRD peaks of PZT.

Figure 2 shows the P–E loop of the Pt/PZT/TiO_2/p-Si(100) structure, indicating a nonsaturating P–E behaviour with a small remanent polarization ($\sim$0.9 μC cm^{-2}). This feature is ascribed to the fact that because of the very large dielectric constant of PZT, the capacitance of the ferroelectric layer is much larger than that of the insulator layer, therefore, the electric field in PZT is too small to make the P–E hesteresis loop sufficiently saturate. This result is similar to those reported using the Au/$SrBi_2Ta_2O_9$/nitride/Si structure [9] and is consistent with the theoretical analysis [10].

Figure 3 shows a typical curve of the 1 MHz C–V characteristic for the Pt/PZT/TiO_2/p-Si(100) structure. The measurement was performed in the dark and at room temperature. The capacitances were measured with the dc bias voltage from +6 V to −6 V and from −6 V to +6 V with a rate of 85 mV s^{-1}. The clockwise C–V hysteresis loop indicated by arrows in the figure is observed. This suggests that the hysteresis resulted from the switching of the ferroelectric polarization of PZT films, rather than charge trapping. The memory window, i.e. the difference of the bias voltage near the flat band capacitance of the loop, is 2.0 V under the bias condition shown in figure 3. This memory window satisfies the practical application of

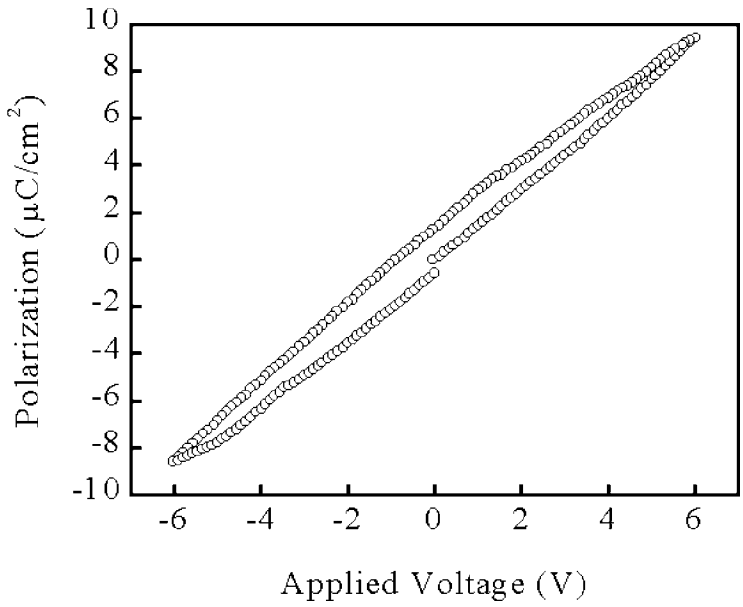

Figure 2. The polarization versus electric-field curve of the Pt/PZT/TiO_2/p-Si(100) structure.

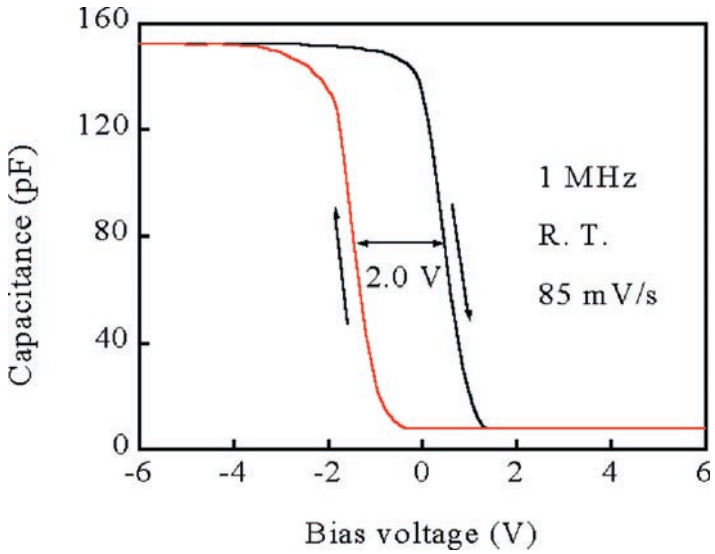

Figure 3. Typical 1 MHz C–V characteristics of the Pt/PZT/TiO_2/p-Si(100) structure.

nondestructive read out (NDRO) ferroelectric random access memories (FRAMs) operating at low voltage [11].

At first sight it may seem hard to understand that such a small remanent polarization could induce such a large memory window. In fact, however, the memory window depends on the coercive electric field applied to the PZT/TiO_2 structure and is insensitive to the remanent polarization. Polarization as small as of the order of 0.1 μC cm^{-2} is enough for controlling the Si surface potential. This is also consistent with the theoretical prediction proposed by Miller

and McWhorter [10].

The current density–voltage (J–V) measurement showed a typical leakage current density of about 10^{-7} A cm^{-2} even at 10 V for the Pt/PZT/TiO_2/Si structure and the fatigue test showed that the C–V memory window remains practically unchanged after 10^7 cycles of switching.

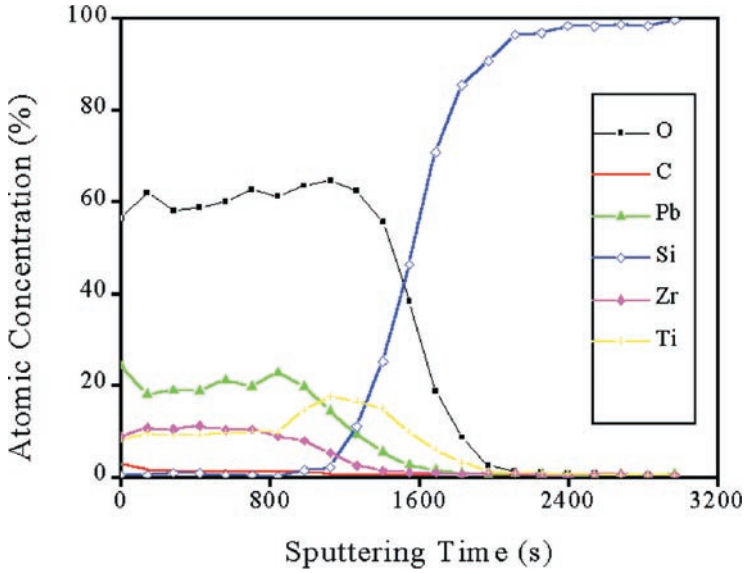

Figure 4. AES depth profiles of Pb, Zr, O, Ti, Si in the PZT/TiO_2/p-Si(100) structure.

Figure 4 shows the depth profiles of constituent elements such as O, Pb, Zr, Ti and Si in PZT/TiO_2/Si structures measured by AES. It can be seen that the interdiffusion of Si atoms into PZT layer and Pb atoms into Si substrates are barricaded by TiO_2 thin films and the PZT/TiO_2/Si structure has a sharp interface microstructure. This result suggests that TiO_2 is a suitable buffer layer for the application of metal/ferroelectric/insulator/semiconductor field effect transistors (MFIS-FETs).

4. Conclusions

We have studied the growth of PZT films on Si substrates with TiO_2 buffer layers using PLD. It was found from the AES measurements that TiO_2 thin films can act as an effective barrier to prevent the interdiffusion between PZT layers and Si substrates. Furthermore, we have demonstrated ferroelectric properties of PZT films grown on Si by using a TiO_2 buffer layer. In the capacitance–voltage (C–V) characteristics of Pt/PZT/TiO_2/p-Si(100) structures, a hysteresis loop with clockwise trace was observed and the memory window was about 2.0 V. Therefore, it can be concluded that the PZT/TiO_2/Si structure prepared in this work is promising for fabrication of ferroelectric FETs.

Acknowledgments

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